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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,877	12/23/1999	ADRIAN SFARTI	0100.9910145	8063

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EXAMINER
PAN, DANIEL H

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/471,877	Sfarti et al.
Examiner	**Art Unit**
Pan	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Dec 23, 1999*

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-33* is/are pending in the applica

4a) Of the above, claim(s) *none* is/are withdrawn from considera

5) ☒ Claim(s) *7-13 and 20-27* is/are allowed.

6) ☒ Claim(s) *1-6, 14, 18, 19, and 28-33* is/are rejected.

7) ☒ Claim(s) *15-17* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. Claims 1-33 are presented for examination.

2. Claims 7-13, 20-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 7 recites the limitation "the information" in lines 18-19. There is insufficient antecedent basis for this limitation in the claim. Suggestion : is "the information" referring to the content of the memory or the request itself ? (See also claim 20, line 19).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 14,18,19, 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wandler et al. (5,991,833) in view of Connors et al. (4,152,764).

5. As to claims 1,28, Wandler disclosed a system, comprising t at least :

a) integrating a central processing unit [CPU] with a north bridge [north bridge] on to a single substrate [10] (see col.6, lines 5-7) that the central processing unit [25] is directly coupled to the north bridge via internal bus [17] (see fig.2 [25][50][17]);

b)providing memory access requests from the central processing unit to the north gate at a rate of the CPU (e.g. see fig.2 [CPU Bus 17], see the memory accesses in col.6, lines 17-22);

c)buffering , in the north bridge [50], the memory access requests (e.g. see fig.4 [508][510] see the CPU-memory read/write queues for storing the requests in col.11, lines 55-67, col.12, lines 1-25);

d)processing by north bridge the access requests (see fig.4 [508][510] see the CPU-memory read/write queues for storing the requests in col.11, lines 55-67, col.12, lines 1-25).

6. Wandler did not specifically show his requests were processed at a rate of memory as claimed. However, Connors disclosed a system for processing requests not to exceed at a maximum memory rate (see col.2, lines 13-27, col.5, lines 60-67). It would have been obvious to one of ordinary skill in the art to use Connors in Wandler for processing the request at a memory rate as claimed because the use of Connors could provide Wandler the control ability to adjust to a different access speed of a given memory device, and it could be readily done by configuring the memory access parameters, such as memory width, and read/write cycles, into Wandler, such that the memory requests at a given memory speed could be processed by Wandler, and because

one of ordinary skill in the art should be able to recognize the need of processing the requests at a memory rate as Wandler also taught a retrying cycle for read/write requests if the memory was busy (e.g. see col.3, lines 22-30) which was a suggestion of processing the request at the speed condition of the memory, and thereby allowing the bus to be freed for access cycles for other devices, and in doing so, provided a motivation.

7. As to claim 2, Wandler also included at least :

a)integrating he south bridge on the substrate with CPU and north bridge (e.g. see PCI bus in fig.2, see also col.6, lines 5-7 for integrating the north bridge into CPU);

b)buffering the requests in the north bridge (e.g. see the request received by north bridge from south bridge in col.12, lines 11-13, col.13, lines 26-43) from south bridge.

8. As to claim 3, Wandler's north bridge [50], CPU and the memory were also integrated on a substrate (e.g see the integrated feature of the north bridge 50 to memory and CPU in col. 6, lines 1-27).

9. As to claim 4, Wandler also included graphic controller [60] for requesting data to the north bridge at graphic controller's rate (e.g. see the rapid retrieval of he data in col.6, lines 28-52).

10. As to claim 14, Wandler also included at least :

a) memory that is contained in substrate [10] (see fig.2);

b)north bridge [50] operably coupled to interface with memory [75] , wherein the north bridge included a memory access request buffer(see fig.4) interoperably coupled with a memory controller [504] (fig.4), wherein the memory access request buffer received memory access request (e.g. see the read/write queues 508 510 in col.11, lines 60-67, col.12, lines 1-10), wherein the memory controller retrieve the request from the buffer (e.g. see the read/write queues 508, 510,512,514 in col.11, lines 60-67, col.12, lines 1-10) and processed the request;

c)memory bus [27] coupled to the north bridge [50] (e.g see fig.4).

11. Wandler did not specifically show retrieving the request at the memory rate as claimed. However, Connors disclosed a system for retrieving memory access requests at a memory speed not to exceeding a maximum memory rate (see col..2, lines 13-27, col.5, lines 60-67). It would have been obvious to one of ordinary skill in the art to use Connors in Wandler for retrieving the request at a memory rate as claimed because the use of Connors could provide Wandler the control ability to adjust to a different access speed of a given memory device, and it could be readily done by configuring the memory access parameters, such as memory width, and read/write cycles, into Wandler, such that the memory requests at a given memory speed could be processed by Wandler, and because one of ordinary skill in the art should be able to recognize the need of processing the requests at a memory rate as Wandler also taught a retrying cycle for read/write requests if the memory was busy (e.g. see col.3, lines 22-30) which was a suggestion of processing the request at the speed condition of the memory, and thereby allowing the bus to be freed for access cycles for other devices, and in doing so, provided a motivation.

12. As to claim 18, Wandler also included PCI bus (e.g. see fig.2 PCI).

13. As to claim 19, Wandler also included a device bus (e.g. see fig.2 connection to peripheral device).

As to claim 29, Wandler also buffering the request by the north bridge 50 from south bridge (see fig.4).

As to claim 30, Wandler also integrating the CPU , north cridge and south bridge (see PCI bus in fig.2, see also col.6, lines 5-7 for integrating the north bridge into CPU).

As to claim 31, Wandler also included graphic controller [60] for requesting data to the north bridge at graphic controller's rate (e.g. see the rapid retrieval of he data in col.6, lines 28-52).

14. Claims 5,6, 32,33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wandler et al. (5,991,833) in view of Connors et al. (4,152,764) as applied to claim 1 and clam 28 above, and further in view of Onishi et al. (5,845,329).

15. As to claims, 5,6, 32,33, neither Wandler nor Connors specifically show the translation of the virtual to physical address of the request as claimed. However, Onishi disclosed a system translating a virtual address into physical address of a memory request (e.g. see col.10, lines 4-13). It would have been obvious to one of ordinary skill in the art o use Onishi in Wandler for translating the virtual and physical address as claimed because the use of Onishi could enhance the processing capability of Wandler to adjust to particular requirements of the memory access at a predetermined format, such as virtual and physical addresses, and it could be readily done by

predefining the translation variables, such as address range of the read/write operation, of Onishi into Wandler's configuration file such that the mapping of the virtual and physical addresses could be recognized by Wandler, and because one of ordinary skill in the art should be able to recognize the need for converting the virtual and physical addresses as Wandler also taught that his memory was a DRAM type memory (col.6, lines 21-27), which was a storage of a physical address array, and in doing so , provided a motivation.

16. As to claims 7-13, 20-27, claims 7-13, 20-27 would be allowable over the art of record for specifically showing the combined features of the functional elements of the instruction module, cache modules , decoder and phase locked loop and the memory access request received from the central processing unit at operational rate of the central processing unit and the memory access request received from the request buffer at the memory rate, the memory access request when information relating to executing one of the operational instructions was not stored in the data module or the instruction module and if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

17. Claims 15-17 are objected for specifically reciting the combined elements of the data module, instruction module, phase locked loop the request issued at the operating rate of the CPU, the memory access request when information relating to executing one of the operational instructions was not stored in the data module or the instruction module and as being dependent

upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan, Esq. whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:00 AM to 4: 00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Chan, can be reached on (703) 305 9712 . The fax phone number for the organization where this application or proceeding is assigned are

a)703 746 7239

b) 703 746 7238

c) 703 746 7240.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305 3900.

DANIEL H. PAN
PRIMARY EXAMINER
GROUP